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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,223	11/20/2003	Kanti Jain	A304	9012
7590 07/21/2005			EXAMINER	
Anvik Corporation 6 Skyline Drive Hawthorne, NY 10532			HEALY, BRIAN	
			ART UNIT	PAPER NUMBER
			2883	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/718,223

Applicant(s)

JAIN ET AL.

Examiner

Brian M. Healy

Art Unit

2883

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-27 is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-9 is/are rejected.
- 7) ☒ Claim(s) 4 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____

DETAILED ACTION

Allowable Subject Matter

Claims 10-27 are allowed. The closest prior art of record, Horie, U.S.P. No.5,511,142 is discussed below. Neither Horie 142' or any other prior art reference teaches or suggests the claimed photonic-electronic multiple layer circuit including depositing and pattern etching TIR complementary photoresist layers to form a rounded channel corresponding to that of an optical fiber. In addition, none of the prior art references teaches the method steps to making a photonic-electronic circuit package including depositing, patterning and developing photoresist layers to leave a slope sided run of a photoresist, depositing waveguide filling material, depositing protective masking layer and etching to leave a ridge waveguide with rounded terminations (see claims 10-27 for specific and additional limitations).

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Neither Horie or any of the prior art references of record teaches or suggests the additional use of embedded photonic bandgap devices in a multi-layer photonic-electronic circuit package (claim 4).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Horie et. al., U.S.P. No. 5,511,142.

Horie et. al. 142' teaches (Figs 67-68) a photonic-electronic multiple layer circuit package having plural optical waveguide intralayers 82 and electronic intralayers 95 formed as directional couplers/switching/modulating devices (Note the gaps between waveguides) with the electronic intralayers being formed in predetermined patterns (Note connectivity to operational elements 96) in order to allow for unobstructed propagation or switching of optical signals. Horie et. al. 142' also teaches (Figs. 97-98) the use of embedded diffractive devices 184, 185, 182 for optical signal modulation. The teaching of Horie et. al. 142' clearly, fully meets Applicant's claimed limitations.

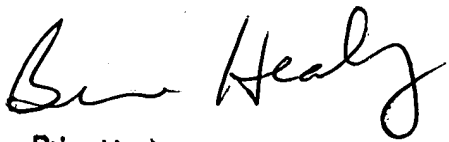
The following references are also cited by the Examiner as being pertinent prior art: Mannschke, U.S.P. No. 4,878,728 (Figs. 1-3), Lackritz et. al., U.S.P. No. 6,724,968 (Figs. 1-12) and Sakata et. al., U.S.P. No. 5,140,149 (Figs. 1-25).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian M. Healy whose telephone number is (571)272-2347. The examiner can normally be reached on Compressed schedule Tues.-Thurs. 7AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (571)272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian M. Healy
Primary Examiner
Art Unit 2883



Brian Healy
Primary Examiner